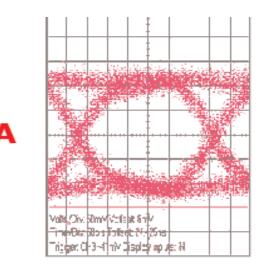


Compliance Specifications from 1.0a to 1.1

From these eye diagrams, can you tell which device is good?



Volts/Disv SumV/Voltset 20/g/V
Time/Disv Sliges Trofset 28 | firs
Trigger CFD = 0/g/V Display Inpute: IN

Most people choose "A"

In the above samples, the rise edge and fall edge distortion on "B" is bigger than "A", therefore "A" seems like the logical choice. We need to understand, however, that the Eye Diagram is dependent on sample size. According to the PCI ExpressTM 1.1 specification, you need 10^{-12} (14 σ) reliability or 10^{12} sample size for interoperability.

Eye Diagrams can not cover everything

Typical eye diagram sample size is only 10^{-4} (3 σ), so it should be considered low level reliability. As you continue to measure jitter, you will realize that the eye opening will actually become closed. This phenomenon is indicated in the formula:

TJ = DJ+nRJ (n : reliability σ)

В

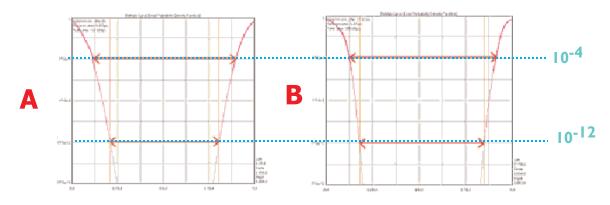
TJ or Jitter pk-pk is composed of DJ and RJ and reliability

Does the PCI Express compliance specification define Interoperability?

The PCI Express1.0a compliance specification did not define interoperability, but rev 1.1 has been changed to include the Interoperability specification.

PCI Express™ Compliance

High Level Device Testing at 10⁻¹²



In the above bathtub plots taken from a BERT, plot "B" shows a better margin than plot "A" at 10^{-12}

Accurate Testing on WAVECREST Signal Integrity Analysis Solutions

WAVECREST's patented jitter separation algorithm, $Tailfit^{TM}$ provides very fast and accurate jitter values including Bathtub plots.

Test Times Meet Production Requirements



SIA-4000 Signal Integrity Analyzer

Sample PCI Express Test Times		
Measurement	Lab	Production
PCI Express 2.5G	1.5s	<100ms
Tr/Tf & Amplitude	1.2s	<90ms
Clock Stats	0.5s	<9ms

PCI Express is a trademark of the PCI-SIG



PCIe AN001_R1a